



# MICROWAVE DIODE RESEARCH

## REPORT NO. 12 THIRD QUARTERLY PROGRESS REPORT

DATE OF THIS REPORT: 10 JUNE 1963  
PERIOD COVERED: 10 DECEMBER 1962 TO 9 MARCH 1963

U.S. Army Signal Research and Development Laboratory  
U.S. Army Supply Agency—Contract DA 36-039 sc-89205  
DA Project No. 3A-99-21-001

Prepared by Bell Telephone Laboratories, Incorporated  
On behalf of Western Electric Company, Incorporated  
222 Broadway, New York 38, N. Y.

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U.S. Army Signal Supply Agency—Contract DA 36-039 sc-89205  
(Continuation of Contract DA 36-039 sc-85325)

DA Project No. 3A-99-21-001

Technical Guidelines—Microwave Diode Research—Dated 16 October 1961

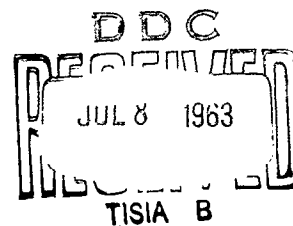
#### OBJECTIVE

*The general objective of this contract is to make theoretical and experimental studies leading toward exploratory models of new microwave crystal diodes.*

#### Authors

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On behalf of Western Electric Company, Incorporated  
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## SUMMARY OF STATUS

Work on this contract is a continuation of that carried out on Contract DA-36-039 sc-85325 and earlier contracts of this continuous series.

During the period covered by this report, 10 December 1962 to 9 March 1963, approximately 1000 man hours were devoted to work on this contract.

Gallium-arsenide (GaAs) varactors of improved cutoff frequency are being made with epitaxial material using nondiffused structures with metal contacts. Zero-bias cutoff frequencies of over 150 Gc are currently achievable, with noise temperatures at 6 Gc in the range 70° K for room-temperature operation.

Noncontract work on metal-epitaxial silicon diodes (Chapter 2) and on high-power protector silicon PIN diodes (Chapters 3 and 4) is reported for collateral interest. The former are good varistor diodes, useful for high-speed logic circuits and probably microwave mixers. Their characteristic response times are too small to measure directly ( $<10^{-10}$  second) and are calculated to be in the range from  $10^{-11}$  to  $10^{-13}$  second. The latter, used as high-power driven switches, are easily able to control 200 kilowatt-microsecond pulses and are calculated to be able to control about 20 megawatt microseconds.

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## SECTION 1 — PURPOSE

This contract continues work previously carried on under Contract DA 36-039 sc-85325.

### Microwave Diode Research

The contractor shall make theoretical and experimental studies leading to fabrication of exploratory models and, upon mutual agreement, to feasibility design and finally development models within the scope of the following:

- (a) New microwave crystal diodes using new or previously untried principles, techniques, or materials.
- (b) New microwave crystal diodes obtained by studied modifications of existing principles, techniques, or materials.

The new diodes shall be primarily intended for and suitable for application to broadband microwave amplifiers, harmonic generators, limiters, and mixers. Major emphasis shall be given to varactor diodes designed to combine refrigerated operation with zero-bias cutoff frequencies well above 100 Gc. High mobility semiconductor materials such as indium antimonide shall be investigated for this purpose. As the scale of effort permits, high-power harmonic generators, high-power limiters, and Esaki diode down-converters of low-noise figure shall be investigated. Particular attention shall be given to development of sound design criteria.

During the course of the contract, the contractor shall deliver, as the state of the art permits, experimental samples having the properties of, and illustrating the circuit applications resulting from, the studies and investigations covered and information on the associated circuitry used for their measurement. The number of experimental samples will be limited in accordance with mutual agreement with the Contracting Officer's Technical Representative. When the data obtained on the experimental samples warrant, and upon mutual agreement between the contractor and the Contracting Officer, development will be undertaken leading to design for production. Upon completion of such design work, the contractor shall deliver suitable additional samples accompanied by engineering drawings and information suitable for fabrication of such samples so that any manufacturer skilled in the art would be able to provide additional samples.

## SECTION 2 — ABSTRACT

In Chapter 1 the use of surface-barrier diodes (also known as metal semiconductor and Schottky diodes) on GaAs is considered. As an experimental vehicle for the measurement of impurity densities, surface-barrier diodes have been used to map the impurity profile in epitaxial GaAs films. Films produced by three substantially different processes have been examined and the results are shown here. Employed as varactors, surface-barrier diodes on epitaxial GaAs are expected to exhibit cut-off frequencies slightly higher than those of diffused diodes. Initial attempts have resulted in zero-bias cut-off frequencies of about 150 Gc and degenerate, 5.85 Gc, noise figures of 1 db.

Chapter 2 discusses a diode based on the properties of an evaporated gold contact on n-type epitaxial silicon that has speeds comparable to point contact diodes. This is possible since the gold-silicon diode has sufficiently low hole injections so that its response time is not governed by minority carriers. The space charge region at zero bias can be designed to penetrate to the impurity tail at the interface, thus reducing series resistance. An encapsulated diode was made with a 1-mil diameter gold contact on an epitaxial layer 1.5 microns thick which had a surface doping of about  $1 \times 10^{15}$  donors per  $\text{cm}^3$ . The RC product of this diode is less than  $1 \times 10^{-12}$  second. Under forward bias, the electron transit time through the epitaxial layer is less than  $2 \times 10^{-11}$  second. The breakdown voltage of experimental diodes is greater than 10 volts. Stress aging experiments in an inert atmosphere show no deterioration of electrical properties at temperatures up to the gold-silicon eutectic ( $370^\circ\text{C}$ ). This diode was used as a harmonic generator at 11 Gc with an efficiency comparable to that of a GaAs point contact diode.

Gold-epitaxial silicon diodes can be designed and fabricated as high speed logic diodes, microwave mixers, varactor amplifiers, or microwave switches.

Chapter 3 discusses a protective switch using a pair of silicon PIN diode wafers mounted in series across a waveguide that has been operated at X-band. The wafers were then unencapsulated, and appropriate tuning elements were required. Over the frequency band between 8.5 and 9.4 Gc, measurements at low signal levels gave protection between 23 and 33 db for the diodes forward biased with 100 ma and insertion loss at zero bias between 0.5 and 0.8 db. The bandwidth was less than 100 mc, so that retuning was necessary when the frequency was changed. The maximum safe incident power was estimated by measuring the temperature rise

in the diode wafers when applying pulses of up to 70 kw power with 2.5 microsecond pulse length. Extrapolation from these temperature rise measurements indicates that for the same pulse length burnout would occur at 15 megawatts incident power.

When these measurements are compared with the performance of gas T-R tubes at X-band (1.0 db low-level loss and 70 db protection over a broad band), it is seen that the PIN switch falls short. However, the results obtained thus far are sufficiently encouraging to justify further development work, especially in view of the expected high power capability and long life of the PIN diode.

As discussed in Chapter 4, a PIN diode bias-driven switch has been tested which gave the following performance: protection greater than 30 db and insertion loss less than 2 db over a 1-Gc band (10.2 Gc to 11.2 Gc). Over a frequency range not coincident with maximum protection, a diode gave less than 2 db insertion loss over a 1.8-Gc band, less than 1 db loss over a 0.5-Gc band, and a minimum loss of 0.6 db. Pulses with 125 kw microsecond pulse energy have been switched by a single diode without burnout. This broad band performance was obtained using a mode of operation, described by Garver (Ref. 1), which is opposite to the switching mode previously used (Ref. 2) in that the relation between diode impedance and bias state is inverted. In the present mode, with the diode mounted across the waveguide, minimum insertion loss is achieved when the diode is forward biased and maximum isolation is achieved when the diode is zero biased. The switching action is based on resonances of the packaged diode alone; external tuning elements are not required. The operating frequency for the switch is controlled in a predictable way by wafer and package electrical parameters.

### SECTION 3 — PUBLICATIONS AND REPORTS

During the period covered by this report, no other reports or publications were issued.

## SECTION 4 - FACTUAL DATA

### Chapter 1

#### METAL-EPITAXIAL GALLIUM-ARSENIDE VARACTORS

By J. C. Irvin

##### 1.1 INTRODUCTION

The metal-semiconductor rectifier has found new application in the development of GaAs varactors. The GaAs surface barrier diode is currently being employed in two distinct roles. It has proven a very convenient experimental tool for the evaluation of epitaxial GaAs films and at the same time shows promise as a practical varactor. In this chapter the results of experiments with GaAs surface-barrier diodes in both functions will be presented. Section 1.2 gives the impurity profiles of three different epitaxial GaAs films as obtained with the help of surface-barrier diodes. A basic difference between the density distributions is noted and its possible origin is discussed. In section 1.3, the predicted performance of an epitaxial GaAs surface barrier varactor is indicated as well as the observed results obtained to date.

##### 1.2 IMPURITY PROFILES IN EPITAXIAL GALLIUM-ARSENIDE FILMS

Zero-bias cut-off frequencies in excess of 500 Gc have been estimated possible for diffused epitaxial GaAs varactors (Ref. 1) and also for epitaxial GaAs surface-barrier varactors (as will be shown later in this chapter). The realization of such performance depends on the accurate control of a number of parameters, the most critical of which are the epitaxial film doping and thickness. The film doping and thickness are determined initially by the epitaxial growth conditions. The thickness may, however, be tailored by etching or allowed for by adjusting the depth of the subsequent diffusion. In either case, it is necessary to know the donor density in the film and its variation with depth in the film. The presence of the low-resistivity substrate prevents impurity concentration determinations by either Hall effect or sheet resistivity measurements. In the absence of these standard techniques, the differential capacity method is frequently employed (Ref. 2 and 3).

For GaAs the net ionized impurity density (in  $\text{cm}^{-3}$ ) is given by

$$|N_d^+ - N_a^-| = 6.35 \times 10^6 \left( \frac{C^3}{A^2} \right) \frac{dV}{dC}$$

where C is in picofarads, V is in volts, and A is in  $\text{cm}^2$ .

Differential capacity measurements on a diode are made by measuring the capacitance, C, and change of capacitance, dC, corresponding to various values of reverse bias, V, and incremental changes in bias, dV. The diameter of the junction must be measured quite accurately since it enters in the fourth power. Likewise, care must be taken to avoid stray capacitances since C appears cubed.

As the dc reverse bias is increased, the boundary of the space charge region extends farther into the epitaxial film. Thus the net donor density may be mapped as a function of depth within the film up to the limit imposed by the breakdown of the diode, which of course depends on the doping. In general the maximum depth allowed by the voltage breakdown is a micron or less, whereas the films may be two or three microns thick. Hence, one or more steps may be etched in the film providing access to donor density determinations at corresponding points within the film.

Use of this method assumes a junction in which the impurity density is much less on one side than on the other, that is, in which the excursions of the space charge region occur almost wholly to one side of the stoichiometric center. A step junction is an especially suitable, though not imperative, choice.

Surface barrier diodes are very desirable for differential capacity impurity determinations for three reasons.

- (a) They are almost ideal step junctions.
- (b) They require no diffusion or alloy-regrowth cycles, treatments which could significantly alter the material being investigated.
- (c) They are readily fabricated.

The result of the application of this technique to three different epitaxial films is shown in Figures 1, 2, and 3. To verify the validity of this method, measurements were also made on a slice of uniformly doped (nonepitaxial) material for which Hall data could be obtained. The correspondence of the two sets of data is shown in Fig. 4.

Film A, shown in Fig. 1, was 1.6 microns thick and had one such step (1.2 microns deep) etched in it. Film B, shown in Fig. 2, was 2.2 microns thick and also had one step etched therein, 1.5 microns deep. Film C, represented by

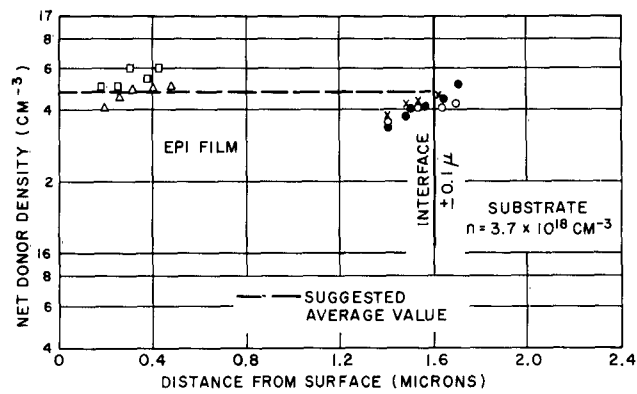


Fig. 1 - Impurity profile of GaAs, epitaxial film A.

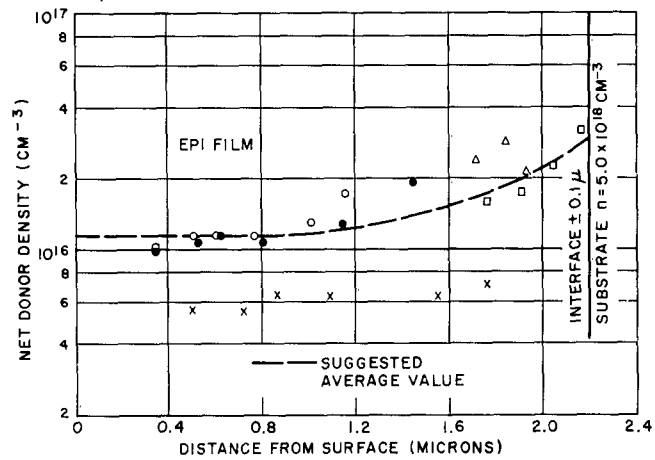


Fig. 2 - Impurity profile of GaAs, epitaxial film B.

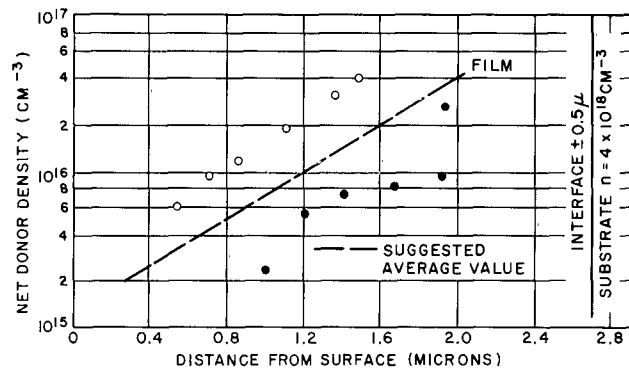


Fig. 3 - Impurity profile of GaAs, epitaxial film C.

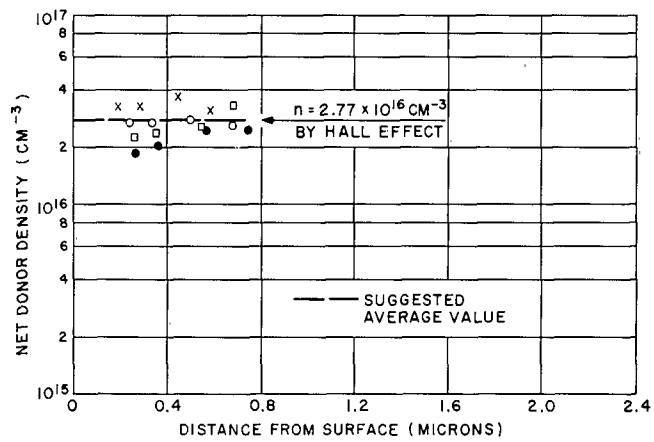


Fig. 4 - Impurity profile in uniform GaAs slice.

Fig. 3, was 2.7 microns thick and was not step etched. An uncertainty of  $\pm 0.1$  micron should be attached to these values.

The primary conclusion to be drawn from Figures 1, 2, and 3 is that the net donor density in films A and B remains essentially constant from the surface down to the substrate interface, whereas in film C the concentration increases from the surface inward. In this connection it should be noted that films A and B, though differing slightly in growth conditions from each other, were both grown at about  $600^{\circ}\text{C}$ , (Ref. 5) whereas film C was deposited at a temperature  $400^{\circ}\text{C}$  higher. Hence it may be speculated that release of and redeposit of donors from the substrate as well as out diffusion from the substrate may be more probable in the case of film C than in the case of films A and B. Such processes are known to be prevalent in the case of silicon epitaxial growth in which case a rapid rise of donor density near the substrate is typical (Ref. 3).

It will also be noted that for each unit of films A and B a slight apparent rise in donor density with depth occurs. This effect may be genuine, though variations of this order may also be ascribed to stray capacitance, surface effects, or other phenomena. The unit in film B (Fig. 2) with significantly smaller apparent doping than the other units in that group was also considerably smaller in diameter and hence subject to greater error in that measurement. Such an error is probably the reason for its dissimilarity.

For device applications, the ideal epitaxial film is one in which the doping transition from substrate to film is very abrupt. Films A and B appear to satisfy this requirement unusually well.

### 1.3 SURFACE-BARRIER VARACTORS

A surface-barrier diode on epitaxial GaAs should be quite similar in performance to the diffused structure discussed previously (Ref. 1). Since the latter design also assumed a step junction, the total capacitance, series resistance, and consequently cut-off frequency,  $F_{co}$ , of both models are nearly the same. The essential difference is the absence of a diffused region and its associated resistance (estimated in Ref. 1 to be only 0.03 ohm) in the surface-barrier varactor. The resultant increase in expected  $F_{co}$  is not important; however other effects derived from the substitution of a surface barrier for a diffused junction may be quite significant.

For operation at liquid nitrogen and especially at liquid helium temperatures, all portions of a varactor outside the space charge region must be doped to degeneracy. The relatively low doping level at which this occurs in n-type GaAs is one of its many attractive assets. However, the required doping in p-type GaAs is higher.



Furthermore, all diffused junctions inherently involve a transition region of impurity density which in practice is rarely a perfect step function. Hence, though degeneracy may prevail on both sides of a diffused junction, a nondegenerate lamina near the space-charge region is apt to exist which could lead to degradation of performance at very low temperatures. The more nearly ideal step junction obtained with surface barriers also enhances the capacitance variation and dynamic Q.

Another peculiarity of the surface barrier (in the case of the gold-GaAs system) is the absence of injection from metal to semiconductor when it is forward biased. This property has plagued efforts to perfect a GaAs transistor but may be a boon to low-noise varactor diode amplifiers. This would be the case if the postulate is correct that injected carriers avalanche under certain conditions and thereby produce excess noise.

A final virtue of the surface barrier diode for device applications is its obviation of high temperature alloying or diffusion processes with their concomitant hazard of adulterating the epitaxial film.

The primary shortcoming of a surface barrier varactor is also related to temperature. Since the surface barrier is not an alloyed junction, alloying temperatures must be avoided (in the neighborhood of 350°C for gold). This prohibition places severe restrictions on packaging, baking, and step-stress aging operations. Because relatively low temperature bonding and sealing methods must therefore be employed, high reliability may be difficult to obtain.

Fig. 5 shows the expected zero-bias cut-off frequency of an epitaxial GaAs surface-barrier varactor for various mesa diameters and epi film dopings under the following set of assumptions:

- (a) A substrate resistivity of 0.0007 ohm-cm
- (b) A total contact resistance of 0.1 ohm
- (c) An epitaxial film electron mobility of 3000 cm<sup>2</sup> per volt-sec
- (d) A uniform doping of the epitaxial film from surface to substrate and also uniform mobility

The third assumption is near reality for currently available epitaxial films in the doping range of interest here. As mentioned earlier, the film thickness is comparable in importance to the doping. Hence two different assumptions are made in plotting Fig. 5. In one case (curves 1 and 2), a total film thickness of 1 micron is assumed; in the other case (curves 3 and 4), a thickness sufficient for a 9-volt space charge region is employed. The first requirement is much less stringent (at higher dopings) than the second, which is similar to that used in Reference 1. The predicted maximum  $F_{co}$  are correspondingly more modest for the film of constant thickness.

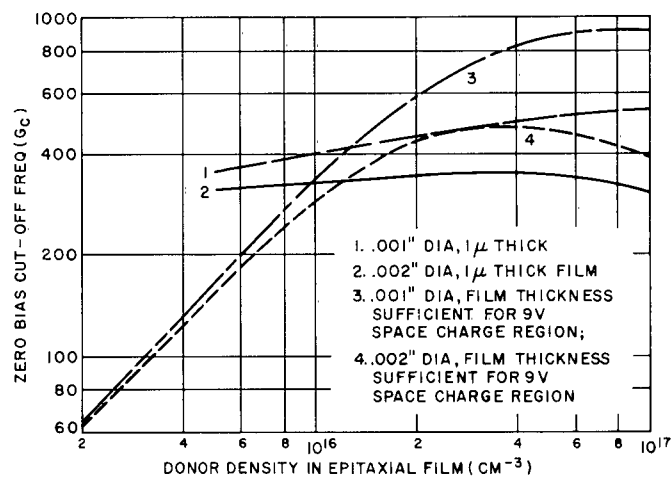


Fig. 5 - Theoretical  $F_{co}$  (zero bias) of epitaxial GaAs surface barrier varactors.

Due to problems arising in the packaging, few surface barrier varactors have been evaluated. Only 3 units have yielded extensive data and these are reported in Table 1-1. The epi film employed in this case was film B, described in section 1.2. Film B, with a thickness of 2.2 microns and donor density of about  $1 \times 10^{16} \text{ cm}^{-3}$ , is far from ideal for the making of high performance (low noise) varactors. The breakdown voltage of these units was about 30 volts. Furthermore, the contacts on these particular units are suspected to be worse than the accepted 0.1 ohm. In view of these unpromising circumstances, the measured  $F_{co}$ ,  $\tilde{Q}$ , and their correspondence with the expected values is considered encouraging. In fact this is one of the few times that observed  $\tilde{Q}$ s have exceeded expectations, probably due to a pessimistic assumption of mobility. Not so pleasant is the discrepancy between expected and observed noise temperature. However, this same situation is usually encountered with diffused varactors as well.

Table 1-1  
THEORETICAL AND OBSERVED CHARACTERISTICS OF EPITAXIAL GaAs  
SURFACE BARRIER VARACTORS

(Based Upon Measured Epitaxial Donor Density of  $1.1 \times 10^{16} \text{ cm}^{-3}$ ,  
Thickness of 2.2 Microns, and Assumed Mobility of  $3000 \text{ cm}^2/\text{volts-sec}$ )

Unit	Measured					Theoretical				
	C <sub>0</sub> (pf)	R (ohms)	F <sub>co</sub> (Gc)	$\tilde{Q}$ (at 5.85 Gc)	T <sub>eff</sub> (°K)	R (ohms)	F <sub>co</sub> (Gc)	$\tilde{Q}$ (at 5.85 Gc)	T <sub>eff</sub> (°K)	
1	0.58	2.16	127	6.4	72	2.35	117	5.3	67	
2	0.77	1.70	122	6.2	78	1.80	115	5.2	69	
3	0.59	2.30	117	5.7	96	2.35	117	5.3	67	

#### 1.4 CONCLUSIONS

Surface barrier diodes have proven effective vehicles for the measurement of donor densities in epitaxial GaAs films. With the aid of this technique, impurity profiles have been mapped in films of different origins. In one case a surprisingly flat profile is observed, whereas in another case a considerable increase in doping is observed with penetration into the film.

A very small number of actual varactors has been fabricated and measured. Zero bias cut-off frequencies around 120 Gc and dynamic  $\tilde{Q}$ s (at 5.85 Gc) of about 6 were measured, which is in good correspondence with the predicted results for these units. The measured effective double channel noise temperatures ranged from 70°K to 95°K in a degenerate 5.85-Gc amplifier with the varactor at room temperature.

## REFERENCES

1. J. C. Irvin, Microwave Solid State Devices, 5th Interim Report, Chapter 3, Contract DA 36-039 sc-85325 (30 August 1961).
2. J. C. Irvin, Microwave Solid State Devices, 8th Interim Report, Chapter 1, Contract DA 36-039 sc-85325 (31 May 1962).
3. C. O. Thomas, D. Kahng, and R. C. Manz, J. Electrochem. Soc., **109**, (November 1962), 1055.
4. J. C. Irvin, Microwave Solid State Devices, Report No. 9, Final Report, Chapters 1 and 2, Contract DA 36-039 sc-85325 (10 September 1962).
5. F. V. Williams and R. A. Ruehrwein, Abs. 141, Electrochem. Soc. Meeting, Detroit (1961).

## Chapter 2

### GOLD-EPITAXIAL SILICON HIGH-FREQUENCY DIODES\*

By D. Kahng and L. A. D'Asaro

#### 2.1 INTRODUCTION

The metal-semiconductor rectifying point contact has long been used for microwave rectification and amplification. This investigation shows that metal-semiconductor diodes can be designed and fabricated by large area techniques for application as microwave mixers or fractional nanosecond switches. In particular, a gold-n-type silicon contact is shown to have a response time governed either by the transit time of electrons through the space charge region or by the RC time. The series resistance is reduced by using an epitaxial structure. It is also shown that since the hole injection is negligibly small in most cases, the response time is independent of hole lifetime. Diodes fabricated by gold evaporation of n-type silicon were found to retain their initial characteristics under stress aging conditions. In this chapter, the design of these diodes will be discussed and the results predicted for the preliminary design will be compared with those obtained by experiment.

#### 2.2 DIODE STRUCTURE AND FABRICATION

The structure is shown in Fig. 6. An epitaxial layer of n-type silicon is grown on an n<sup>+</sup> substrate. A layer of gold is evaporated in a small dot over the epitaxial layer. The metal semiconductor contact formed in this way has an internal potential which results in a space charge region in the silicon near the gold. The doping and thickness of the silicon is chosen so that at zero bias the space charge region of thickness,  $w$ , occupies most of the epitaxial layer. The remaining portion,  $s$ , is a region of high doping due to diffusion of impurities from the substrate (Ref. 1 and Ref. 2). Experimental diodes were fabricated as follows. Silicon wafers of resistivity  $4 \times 10^{-3}$  ohm-cm, and with faces perpendicular to the  $\langle 111 \rangle$  direction, were deposited with epitaxial layers of silicon by the hydrogen reduction of silicon tetrachloride (Ref. 1 and Ref. 3). The technique of deposition

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\*Work reported here was not done under the contract, but is included because of its relevance.

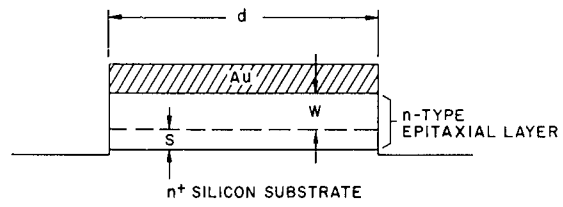


Fig. 6 - Structure of gold-silicon epitaxial barrier diode.

was identical with that described in Reference 1. The film thickness was 1.5 microns. The surface doping of the n-type layers was in the range from  $2 \times 10^{14}$  to  $1 \times 10^{15}$  donors per  $\text{cm}^3$ .

The undeposited side of the wafers were provided with gold-antimony evaporated and alloyed ohmic contacts. These wafers were then subjected to cleaning consisting of oxidation and oxide removal steps. The wafers were cleaned immediately prior to gold evaporation.

Gold evaporation was carried out in a vacuum of less than  $2 \times 10^{-6}$  mm Hg. Gold wire of 99.99 per cent purity was evaporated to a thickness of 10,000 Å through a molybdenum mask which confined the gold in a circular area 1 mil in diameter.

After evaporation, the diodes were etched using the gold dots as masks. The etching removed the epitaxial region outside of the gold dots in order to prevent formation of large area channels near the gold dots.

### 2.3 RESPONSE TIME

The response time is determined by the transit time of majority carriers through the space charge region and the RC charging time. The transit time is given approximately by  $\tau_t = w/v_s$ , where  $w$  is the space charge width and  $v_s$  is the average scattering limited velocity in the space charge region. The RC charging time can be estimated from the resistance of the unswept-out region of the epitaxial layer plus the spreading resistance in the substrate and the capacitance of the contact.

$$RC = \frac{C}{a} \int_{\text{region } s} \rho_e dx + \frac{2C\rho_s}{\pi d} \quad (1)$$

where  $C$  is the capacitance of the diode,  $a$  is the area of the diode,  $\rho_e$  is the resistivity of the epitaxial layer in region  $s$ ,  $\rho_s$  is the resistivity of the substrate, and  $d$  is the diameter of the contact.

Calculation of the response time can be made for a case where the donor distribution in the epitaxial layer is known. In layers a few microns thick, the effect of diffusion from the substrate and the effect of the process on the distribution of impurities (Ref. 1) need to be considered. The doping profile may be characterized by the form (Ref. 1 and Ref. 2).

$$N = \frac{N_s}{2} \operatorname{erfc} \frac{x}{2\sqrt{Dt}} + N_0^* e^{-\phi x} + A(1 - e^{-\phi x}) \quad (2)$$

where the first term is due to diffusion from the substrate of doping,  $N_s$ , with an effective diffusion coefficient,  $D$ , for a time  $t$  (an approximation); the second term is the substrate contribution to the film doping through the exchange of dopant between the solid and gas phase with parameters  $N_0^*$  and  $\phi$ ; and the last term is the gas phase contribution to the film doping with an asymptotic value,  $A$ , for thick films. An example of an impurity distribution obtained in the fabrication of experimental gold-silicon epitaxial diodes is given in Fig. 7. The shapes of the diffusion and exchange contributions to the doping are much larger than the gas phase contribution in the thicknesses used here. Within the lower doped region, an approximation may be made by a uniform doping for estimates of performance.

The width of the space charge region at equilibrium in a uniformly doped material is given by

$$w = \left( \frac{2\epsilon V_D}{qN} \right)^{1/2} \quad (3)$$

where  $\epsilon$  is the dielectric constant,  $V_D$  is the diffusion potential (shown on Fig. 8),  $q$  is the electron charge, and  $N$  is the donor concentration. In a typical case for these diodes, the donor concentration in the region in which the exchange contribution dominates may be  $1 \times 10^{15}$ . The barrier height for the gold-silicon contact ( $V_0$  in Fig. 8) is known from measurements of the forward and reverse characteristics and the capacitance-voltage relation (Ref. 4), and is  $0.79 \pm 0.02$  ev for silicon dopings from 0.1 to 10 ohm-cm. At  $N_d = 1 \times 10^{15}$ , the Fermi level is 0.25 volt below the conduction band, leading to  $V_D = 0.54$  volt and  $w = 0.82$  micron. Since the edge of the space charge region falls in the diffusion tail, the series resistance of the diode is due to the doping in this tail.

The zero bias capacitance can be found from

$$C = \frac{\epsilon}{w} A \quad (4)$$

where  $A$  is the diode area. For a 1-mil diameter diode, the expected zero bias capacitance is about 0.06 picofarad. The capacitance of the encapsulation raises the total to about 0.3 picofarad, making the estimated RC product equal to  $6 \times 10^{-13}$  second for the diodes with a series resistance of 2 ohms.

The transit time of majority carriers through the space charge region at zero bias leads to an upper limit on the response time. For the case given above under zero bias the transit time is about  $2 \times 10^{-11}$  second. Under forward bias, the width of the space charge region decreases and, hence, the response time may be shorter than this estimate.



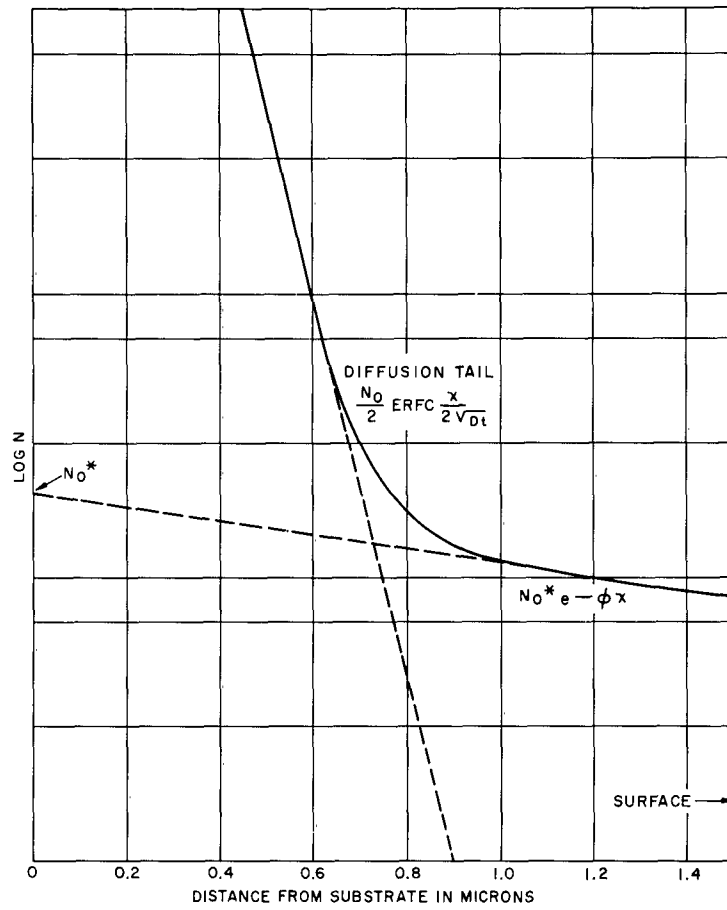


Fig. 7 - Impurity profile components for an epitaxial silicon film.

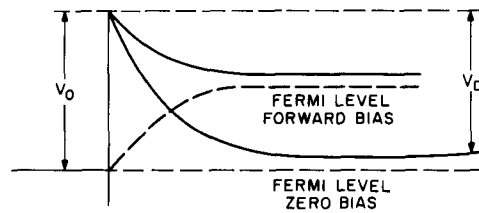


Fig. 8 - Shape of the potential barrier under zero and forward bias.

## 2.4 HOLE INJECTION CONSIDERATIONS

The hole injection ratio is defined as

$$\gamma = \frac{j_p}{j_p + j_n} \quad (5)$$

where  $j_p$  is the hole current and  $j_n$  is the electron current crossing the junction. The hole current is given by diffusion theory as (Ref. 5)

$$\begin{aligned} j_p &= \frac{p_n q D_p}{L_p} (e^{\beta v} - 1) e^{-x/L_p} \\ &= j_{ps} (e^{\beta v} - 1) e^{-x/L_p} \end{aligned} \quad (6)$$

where  $p_n$  is the equilibrium concentration of holes in n-type material,  $D_p$  is the diffusion constant for holes,  $L_p$  is the diffusion length for holes,  $\beta = q/kT$ .  $k$  is Boltzman's constant,  $T$  is the absolute temperature,  $v$  is the externally applied voltage across the junction, and  $x$  is the distance from the metal-semiconductor boundary.

The electron current can be conveniently found from the "diode" theory (Ref. 6) for barriers that are high compared with  $kT$  and for the case when an electron mean free path is longer than the distance within which the barrier changes by  $kT$  near the top of the barrier. These conditions are satisfied for the gold-silicon contact. Then

$$\begin{aligned} j_n &= A T^2 e^{-\beta v_0} (e^{\beta v} - 1) \\ &= j_{ns} (e^{\beta v} - 1) \end{aligned} \quad (7)$$

where  $A$  is a constant with units of ampere/cm<sup>2</sup> · degree<sup>2</sup>. For cases where  $j_p \ll j_n$ ,  $j = j_n$  can be used. Then  $\gamma = j_{ps}/j_{ns}$  and

$$\gamma = \frac{q D_p p_n}{L_p j_{ns}} \quad (8)$$

For  $N_d = 1 \times 10^{15}$  and the experimental values of  $A$  ( $\approx 40$ ) and  $v_0$  ( $\approx 0.79$  ev) from Reference 4,  $\gamma \approx 1 \times 10^{-7}$  is obtained. In most cases the hole injection will not have a significant effect on the response time. In the case of sufficiently large forward currents the above analysis may not be applicable.

## 2.5 BREAKDOWN VOLTAGE

The avalanche breakdown voltage can be estimated from the known ionization rate of electrons (Ref. 7). At breakdown,

$$\int_0^w \alpha \, dx = 1 \quad (9)$$

where  $\alpha$  is the ionization rate. The electric field dependence is empirically described by

$$\alpha = ae^{-b/E} \quad (10)$$

where  $a$  and  $b$  are constants.

For the case of the epitaxial layer where the space charge region terminates on heavily doped substrate material, the electric field may be taken as constant. Then since

$$\int_0^w \alpha \, dx = aWe^{-b/E} = 1 \quad (11)$$

one obtains

$$V_B = \frac{bw}{\ln aw} \quad (12)$$

where  $w = 0.8$  micron and  $V_B = 34$  volts. This estimate may be subject to some error since Reference 7 does not consider microplasma effects. Experimental diodes show breakdown voltages which approach and occasionally exceed this value.

## 2.6 ELECTRICAL MEASUREMENTS

A group of experimental diodes showed the properties given in Table 2-1.

Table 2-1  
PROPERTIES OF EXPERIMENTAL  
DIODES IN ENCAPSULATIONS

Diode	$V_B$ at 10 $\mu$ amp (volts)	$C_o$ (pf)
D31	22	0.26
D32	12	0.26
D35	13	0.27
D37	25	0.29

The capacitance was measured at zero bias. These diodes show a forward V-I characteristic given in Fig. 9. Often the forward characteristic can be approximately described by the empirical relation.

$$I = I_s \exp \frac{q}{nkT} (V - IR) \quad (13)$$

in which  $n$  is an empirical constant and  $R$  is the current independent series resistance. The "diode" theory predicts the forward characteristics of the form of Eq. (13) with  $n = 1$ . The departure of  $n$  from unity is sometimes attributable to currents generated at traps within the space charge region (Ref. 4). Experiments on diodes of larger diameter show that these traps are located around the periphery of the diode at the gold-silicon interface. In general  $n$  is a continuously varying quantity with the current. Equation (13) would not apply for the high current density regions since the "diode" theory fails to yield satisfactory predictions. One possible high current density effect is increased minority carrier injection. This would cause  $R$  to vary with the current also. Characteristics of other diodes normalized to 1-mil diameter mesas are given for comparison in Fig. 9.

## 2.7 RESPONSE TIME MEASUREMENTS

The response time of the experimental diodes was examined by a pulse recovery measurement. No storage time as large as the resolving time of the equipment, which is 1 nanosecond, was found.

A further measurement of an experimental diode was made by A. F. Dietrich who used a method previously described for generating carrier pulses at a frequency of 11 Gc (Ref. 8). In this method the RF pulses are generated directly from the harmonics of the envelope frequency that is found at the beginning or the end of the pulse transient of the diode. The power output at 11 Gc was comparable to that previously obtained with a silicon snap-back diode (FD-100) or a GaAs point contact diode. These results indicate that the response time of the diode under forward bias may be less than  $1.5 \times 10^{-11}$  second.

## 2.8 STRESS AGING EXPERIMENT

Two groups of eight diodes were subjected to stress aging in an effort to establish the expected reliability of the gold-silicon contact. These diodes were mounted on the same header in order to provide an equal stress condition but were not encapsulated. Heating the first group for one-hour periods at increasing temperature steps up to the gold-silicon eutectic temperature (370°C) produced no significant degradation in their forward or reverse characteristics. The second group of eight diodes was heated at 360°C for 64 hours. These diodes also showed no

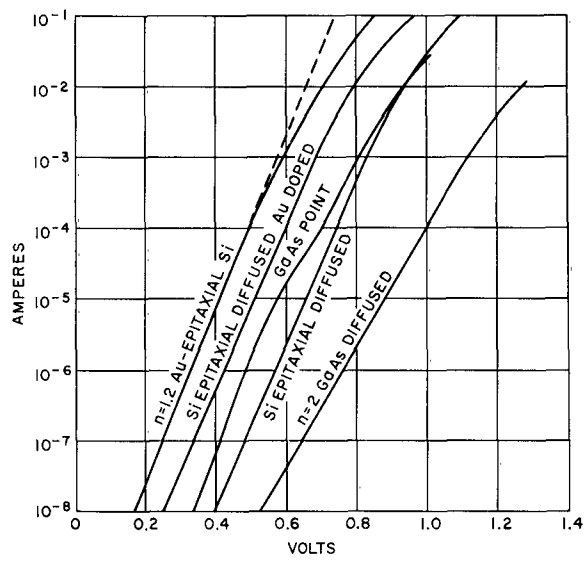


Fig. 9 - Forward bias voltage-current characteristics of a gold-epitaxial silicon diode in comparison with other diodes. (Diode diameters are 1 mil except for the GaAs point contact. The dotted line has a slope of  $n = 1.2$ ).

significant degradation in their V-I characteristics. These experiments indicate that the gold-silicon contact can probably be made adequately stable for device use in a suitable encapsulation.

## 2.9 CONCLUSIONS

The preliminary design described above has been found to yield experimental devices which are sufficiently fast and stable to be useful as computer diodes or as microwave mixer diodes. Another design in which the space charge region penetrates part way through the epitaxial layer may also be of interest as a varactor. It may be expected that the large area techniques used in the design and fabrication of these diodes will lead to more reproducible and stable devices than point contact diodes with similar frequency response.

## REFERENCES

1. C. O. Thomas, D. Kahng, and R. C. Manz, J. Electrochem. Soc., **109** (1962), 1055.
2. D. Kahng, C. O. Thomas, and R. C. Manz, J. Electrochem. Soc., **109** (1962), 1106.
3. H. C. Theurer, J. Electrochem. Soc., **108** (1961), 649.
4. D. Kahng, "Conduction Properties of the Au-n-type Silicon Schottky Barrier," IRE-AIEE Solid State Device Research Conference, University of New Hampshire, July, 1962, also to be published in Solid State Electronics.
5. H. K. Henisch, Rectifying Semiconductor Contacts, (Oxford University Press, 1957), 229.
6. H. A. Bethe, MIT Radiation Lab. Report 43/12 (1942).
7. J. Maserjian, J. Appl. Phys., **30** (1959), 1613.
8. A. F. Dietrich, Proc. IRE, **49** (1961), 972.

## Chapter 3

### PERFORMANCE OF A TUNED PIN DIODE SWITCH AS A PROTECTOR FOR HIGH POWER LEVELS AT X-BAND\*

By D. Leenov and R. C. Swenson

#### 3.1 INTRODUCTION

The silicon PIN diode has been developed for use as a microwave radar protector with high reliability. Both biased and unbiased operation have been shown to be feasible. This report describes experiments carried out to determine whether PIN diode switches can satisfy the requirements on X-band protectors now being met by T-R tubes (70-db protection and 1.0-db low-level loss over a broad band). A switch consisting of a pair of silicon PIN diode wafers, each 0.050 by 0.050 by 0.007 inch mounted in series across a wave guide, was tested. The results obtained, 23 to 33 db protection at forward bias and 0.5 to 0.8 db low-level loss at zero bias, do not meet these requirements but are sufficiently encouraging to justify further work. From measurements of temperature rise as a function of incident microwave power, it is estimated that burnout would occur at incident pulse energies of 38 megawatt-microseconds, which is in good agreement with theoretical predictions.

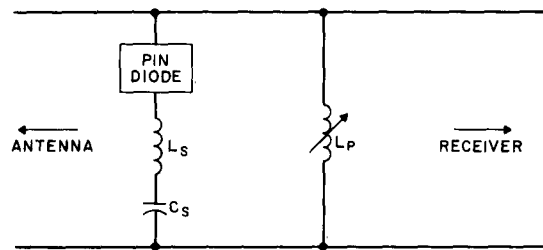
#### 3.2 THEORY OF SWITCH ACTION

The switching action of the PIN diode results from the fact that its microwave impedance is a function of dc bias. At zero bias the diode wafer acts as a capacitance  $C_D$  with a small series resistance  $R_s$  (of the order of a few ohms); at sufficient forward bias (more than a few ma) it acts as a small resistance,  $R'_s$  (of the order of one ohm or less). A switch consisting of a PIN diode shunting a transmission line is shown schematically in Fig. 10a. The tuning capacitance  $C_s$  is used to tune the lead inductance  $L_s$  at the operating frequency. At zero bias (Fig. 10b), maximum transmission is obtained by adjusting the shunt tuning inductance  $L_p$  to resonate with  $C_D$ ; the insertion loss is then due to  $R_s$  and is given by

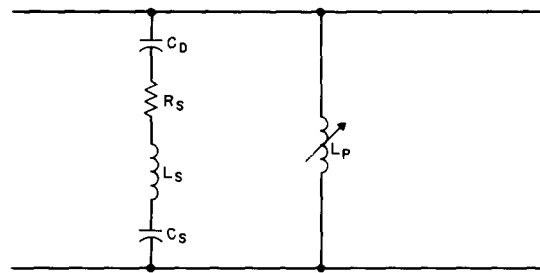
$$(I. L.)_{\min} = \left( 1 + \frac{1}{2} \omega^2 C_D^2 R_s Z_0 \right)^2 \quad (1)$$

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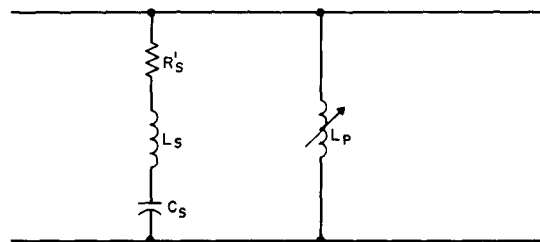
\*Work reported here was not done under the contract but is included because of its relevance to the project.



(a) Schematic



(b) Zero-bias equivalent



(c) Forward-bias equivalent

Fig. 10 - PIN protector switch



where  $Z_0$  is the line impedance and  $\omega$  is the signal angular frequency. At forward bias, the line is shunted by the small resistance  $R'_s$  (Fig. 10c) and the isolation at band center is given by

$$(I. L.)_{\max} \cong \left( \frac{Z_0}{2R'_s} \right)^2 \quad (2)$$

The incident power level required to burn out the protector diode is given by (Ref. 1)

$$P_{\max} = \frac{Z_0}{4R'_s} P_b = 2000 \text{ watts} \quad (3)$$

(where  $P_b$  = diode burnout power  $\cong 20$  watts,  $Z_0 \cong 400$  ohms, and  $R'_s = 1.0$  ohm) for CW signals or for pulses longer than the thermal relaxation time of the diode wafer (8 milliseconds). For short pulses the maximum incident pulse energy  $W_{\max}$  is given by (Ref. 1)

$$W_{\max} = \frac{Z_0}{4R'_s} W_b = 39 \text{ megawatt-microseconds} \quad (4)$$

when  $Z_0 = 400$  ohms,  $R'_s = 1.0$  ohm, and  $W_b$ , the pulse energy for burnout, is of the order of 0.39 watt-second for the diodes used.

### 3.3 DESCRIPTION OF DIODE MOUNT

To contact the diode wafers with minimum lead inductance, a diaphragm extending across the entire guide and from the top to within 0.050 inch of the bottom was used. A pin extending from the bottom of this diaphragm contacted the wafers (unencapsulated to eliminate package parasitics) mounted on a second pin extending through a hole in the bottom of the guide. This pin was mounted on the central conductor of a coaxial trap designed to present the value  $C_s$  required for the tuning capacitance. The shunt tuning inductance  $L_p$  was obtained with two adjustable vanes sliding between the bottom of the diaphragm and the bottom of the guide and held in place by appropriate slots. These tuning devices were quite similar to those which have been used successfully at a lower frequency (Ref. 2). To minimize low-level insertion loss, additional tuning was necessary and was accomplished with slide screw tuners placed on each side of the diode mount.

### 3.4 MEASUREMENTS: METHODS AND RESULTS

The performance of the PIN switch at low power levels was measured by first adjusting the tuning elements to maximize transmission for the zero-biased diode; the insertion loss was then measured. Next the diode was forward biased and the isolation was measured without changing the tuning. The resulting data are plotted in Fig. 11. The measured values of protection are about 30 db (considerably less than the 70 db of T-R tubes). The low level insertion loss values (less than one db) are competitive with T-R tubes, but because of the low protection a practical protector might require more than one stage, which would mean greater low-level loss. Thus, improvement in protection or low-level loss (or both) is required.

A measurement of bandwidth for low-level insertion loss was made by observing the change in frequency required to increase I. L. by one db with the tuning elements unchanged. The bandwidth was found to be in the neighborhood of 100 megacycles or less.

The high-level measurements consisted of a determination of temperature rise  $\Delta T$  in the forward-biased diode as a function of incident pulse energy. To make temperature rise measurements, the diode was calibrated as a thermometer by measuring forward voltage drop versus temperature while a constant bias current was applied. The instantaneous temperature rise produced by each microwave pulse was determined by measuring the instantaneous voltage change indicated on an oscilloscope screen. A plot of  $\Delta T$  versus incident peak power (pulse length constant) is seen to be quite linear (Fig. 12). Extrapolation to a temperature rise of 350°C (corresponding to burnout for these wafers) indicates that for pulses of this length (2.5 microseconds) burnout would occur at about 15 megawatts.\*

This corresponds to a value of 38 megawatt-microseconds for maximum incident pulse energy, which is in good agreement with the theoretical prediction (Eq. 4).

### 3.5 CONCLUSIONS

A PIN protective switch has been operated at X-band and indications of high power capability have been obtained. Values of minimum insertion loss, maximum isolation, and maximum safe power level are sufficiently promising to indicate the feasibility of developing a practical PIN protector. However, the present design has the following disadvantages: absence of diode encapsulation, inconvenient mounting arrangement, need for external tuning adjustments which result in complicated

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\*This extrapolation assumes uniform heating, that is, the absence of hot spots at higher power levels.

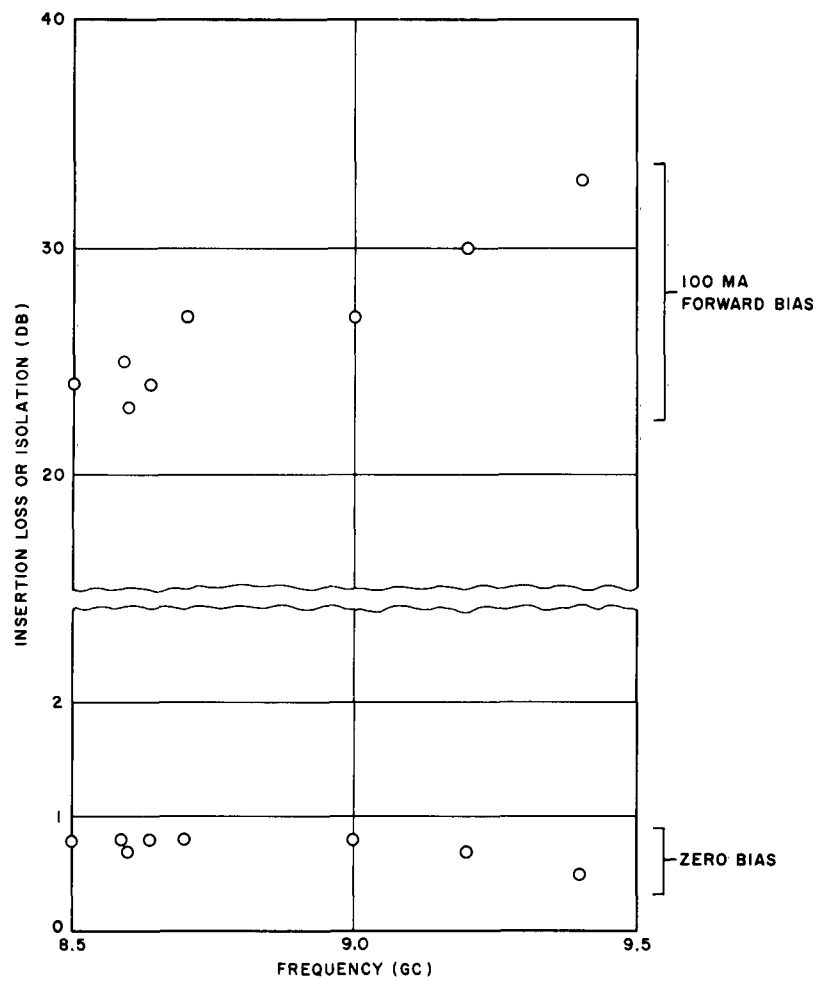


Figure 11. Insertion loss at zero bias and isolation at 100-ma forward bias, as functions of frequency measured at low power levels.

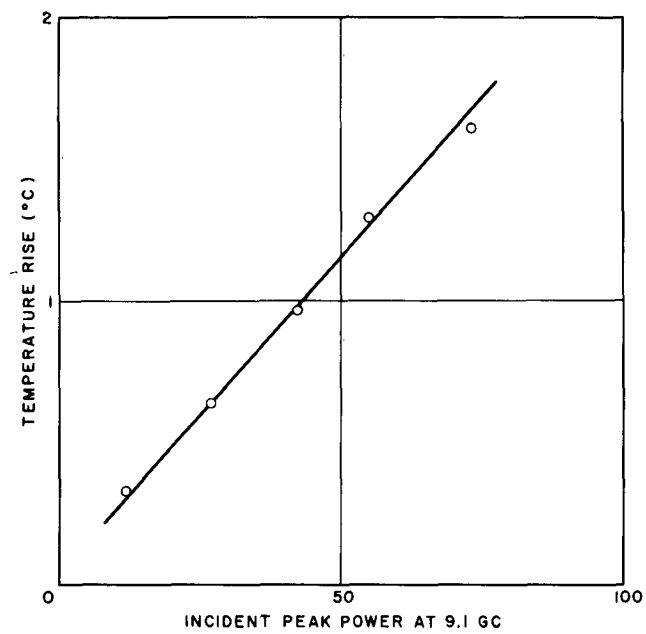


Figure 12. Temperature rise versus high level incident power at a frequency of 9.1 Gc; diode biased at 100 ma.

hardware, and narrow bandwidth. The possibility of overcoming these disadvantages is indicated by a different mode of operation described in the following chapter.

#### REFERENCES

1. D. Leenov, "The Silicon PIN Diode as a Microwave Radar Protector at Megawatt Levels: Theory," First Quarterly Report on Microwave Diode Research, Signal Corps Contract DA-36-039-sc-89205 (December 10, 1962).
2. M. R. Barber, private communication.

## Chapter 4

### BROADBAND PIN DIODE SWITCH OPERATING AT X-BAND WITHOUT EXTERNAL TUNING\*

By D. Leenov

#### 4.1 INTRODUCTION

The complexity of p-n junction microwave switches becomes greater with increasing operating frequencies. Thus, in the VHF range, merely an appropriate diode shunting a transmission line will give low loss at zero bias and high loss at forward bias. In the lower UHF range the zero-bias capacitive reactance of the diode is no longer large enough to give low loss, and a shunt resonating inductance must be added. At frequencies of about 1 Gc or greater, the lead inductance must be tuned by series capacitance to achieve high loss at forward bias. Finally, at X-band the effects of package parasitics (series inductance and shunt capacitance) tend to invert the basic switching function of the diode itself (high zero-bias impedance and low forward-bias impedance).

The X-band PIN switch described previously (Ref. 1) was made to operate in the basic mode just described by using unencapsulated wafers in a specially designed waveguide. While the measured values of insertion loss and isolation represented a promising start, the switch had a narrow bandwidth. Broadband performance with an encapsulated diode has been obtained using what Garver (Ref. 2) termed mode-2 switching. In this mode of operation, high loss is obtained when the diode is zero biased due to series resonance between diode capacitance and lead inductance, and low loss is obtained at forward bias due to shunt resonance between lead inductance and package capacitance. Minimum transmission loss and maximum isolation can be obtained over the same frequency band by proper choice of diode wafer capacitance or of package parasitics. Measured values of low-level loss and maximum isolation are not yet competitive with gas tube protectors, for example, but improvements are expected from proper choice of wafer and package parameters.

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\*Work reported here was not done under the contract, but is included because of its relevance.

## 4.2 THEORY

In mode 2 switching, the high-loss (OFF) state is due to series resonance of diode wafer capacitance  $C_d$  and package inductance  $L_c$ , and the low loss (ON) state is due to shunt resonance of  $L_c$  and package capacitance  $C_c$ . For the high loss condition (maximum isolation), the diode is zero biased; maximum insertion loss then occurs at the resonant frequency for  $C_d$  and  $L_c$  (Fig. 13a):

$$f_1 = \frac{1}{2\pi\sqrt{L_c C_d}} \quad (1)$$

and is given by

$$(IL)_{\max} = \left( \frac{Z_0}{2R_s} \right)^2 \quad (2)$$

since the transmission line (of impedance  $Z_0$ ) is shunted by the low resistance  $R_s$ . Thus  $f_1$  is approximately the central frequency of the band for maximum isolation. For the low-loss condition (maximum transmission), the diode is forward biased so that its impedance becomes a low resistance  $R'_s$  (Fig. 13b); minimum insertion loss then occurs at the resonant frequency for  $L_c$  and  $C_c$

$$f_2 = \frac{1}{2\pi\sqrt{L_c C_c}} \quad (3)$$

and is given by

$$(I. L.)_{\min} = \left( 1 + \frac{Z_0 R'_s}{8\pi^2 f_2^2 L_c^2} \right)^2 \quad (4)$$

It is evident that maximum isolation and minimum insertion loss will occur over the same band when

$$C_d = C_c \quad (5)$$

This desired result can be obtained by control of either of the capacitances in Eq. (5). Appropriate choice of  $L_c$  then determines the frequency band of operation.

The simple theory described above may be used to predict the major properties of switch operation. For example, for the high-loss state Eq. (1) predicts that the central frequency is a function of diode capacitance  $C_d$  and hence depends on wafer dimensions. The maximum insertion loss, determined by  $R_s$  (Eq. 2), is expected to be relatively unchanged by application of reverse bias in the case of the PINs used thus far. These diodes have high-resistivity  $\pi$  layers with low loss

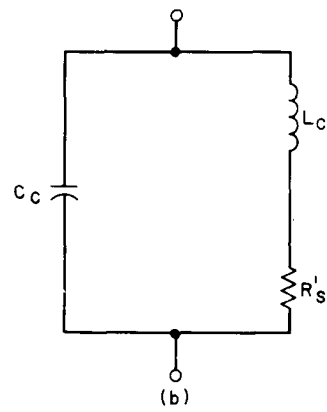
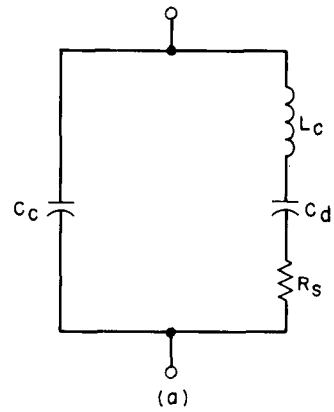


Figure 13. Electrical equivalents of diode wafer and package  
 a. Zero bias  
 b. Forward bias.



at X-band frequencies; hence,  $R_s$ , being due mainly to the resistance of the heavily doped  $\underline{p}$  and  $\underline{n}$  regions, is relatively unaffected by reverse bias.

For the low-loss state, Eq. (3) predicts that the central frequency is unaffected by changes in diode wafer dimensions. However, the insertion loss at frequency  $f_2$  (Eq. 4) is bias sensitive; with increasing bias current,  $R'_s$  decreases; hence, the insertion loss is also expected to decrease.

The above predictions are expected to apply at any signal power level at which diode impedance is determined by the dc bias. Thus far they have been verified for power levels up to 50 kilowatts.

#### 4.3 RESULTS OF EXPERIMENT

Experimental data have been obtained to test the above predictions. The variation in frequency  $f_1$  (Eq. 1) with diode capacitance is illustrated by plots of measured values of isolation versus frequency for three values of  $C_d$  (Fig. 14). It is seen that  $f_1$  increases with decreasing  $C_d$  and that peak isolation decreases with increasing diode resistance. (It has also been observed that applying reverse bias produced no change in the value of isolation.)

Insertion loss values are plotted against frequency for three different values of  $C_d$  in Fig. 15. Essentially no variation in central frequency  $f_2$  is observed. The expected decrease in minimum insertion loss with increasing bias current is shown for one diode in Fig. 16.

To illustrate the practicality of constructing a switch with optimum isolation and insertion loss in the same band, a diode, consisting of two series-mounted 10-mil-thick PIN wafers, 0.050 inch by 0.012 inch in cross section was used. This resulted in  $C_d \simeq C_c$ . The data (Fig. 17) indicate isolation  $>30$  db and insertion loss  $<2$  db for 600 milliamperes forward bias, over the band from 10.2 to 11.2 Gc.

To compare performance at low and high power levels, insertion loss and isolation measurements were made over the same band at low level (a few milliwatts) and at high level (40- to 50-kilowatt pulses of 2.5-microsecond length). The results (Fig. 18) are not intended to illustrate optimum performance, but to show that insertion loss and isolation are independent of power up to 50 kilowatts. Incidentally, it was possible to switch the diode repeatedly between the high impedance and low impedance states with the high power on, without burnout of the wafer.

#### 4.4 CONCLUSIONS

A PIN diode switch operating with modest bias current has given isolation greater than 30 db and insertion loss less than 2 db over at least a one-Gc band,

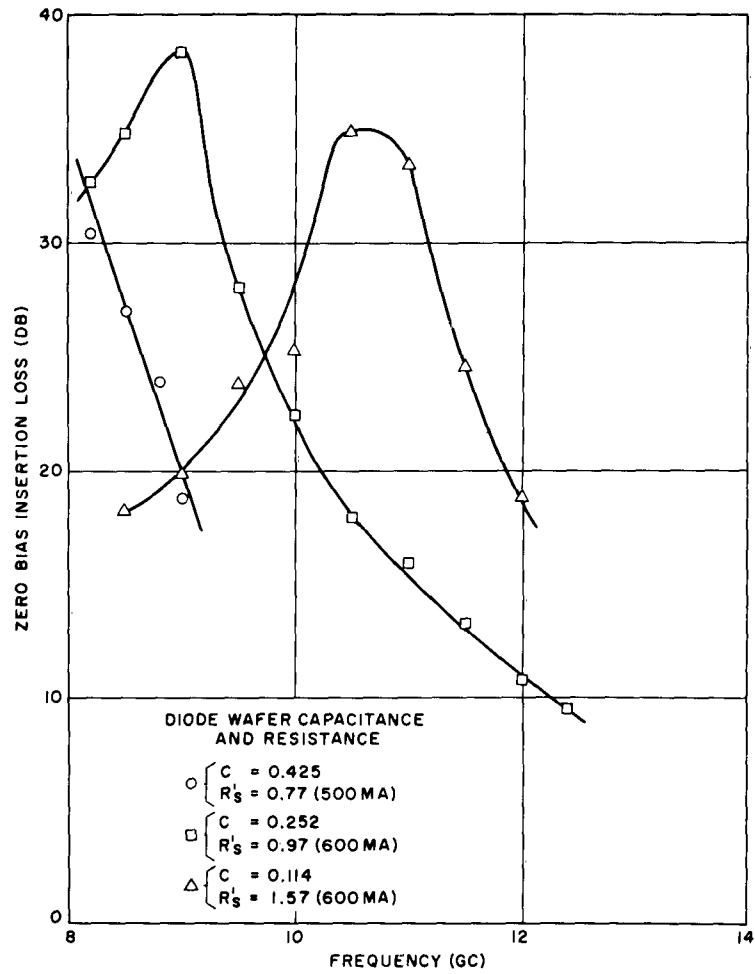


Figure 14. Isolation versus frequency showing increases of resonant frequency with reduced diode capacitance and reduction of maximum loss with increased diode resistance [forward-bias resistances ( $R'_s$ ) are given; zero-bias resistances  $R_s$  are not known accurately].

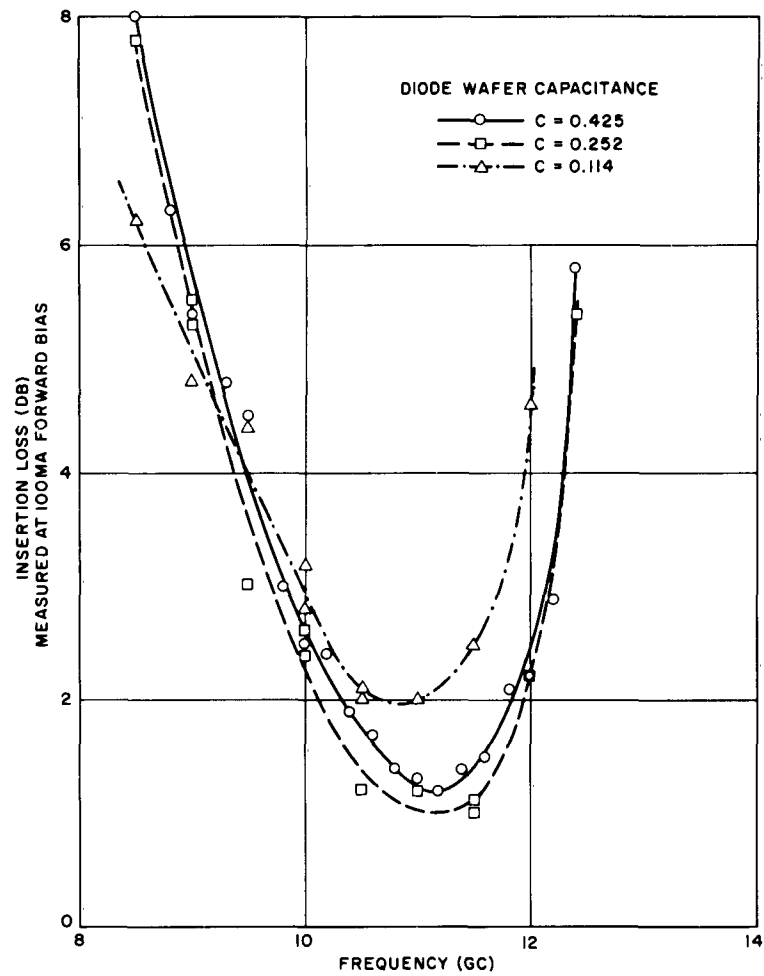


Figure 15. Insertion loss versus frequency measured for diodes of varying wafer capacitance (showing that position of minimum loss is independent of diode parameters).

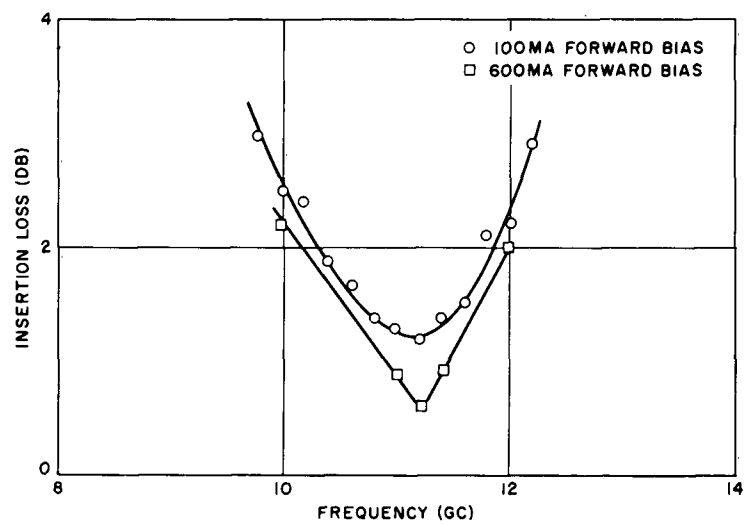


Figure 16. Insertion loss versus frequency measured for two values of bias current (showing reduction in minimum loss with increase in current).

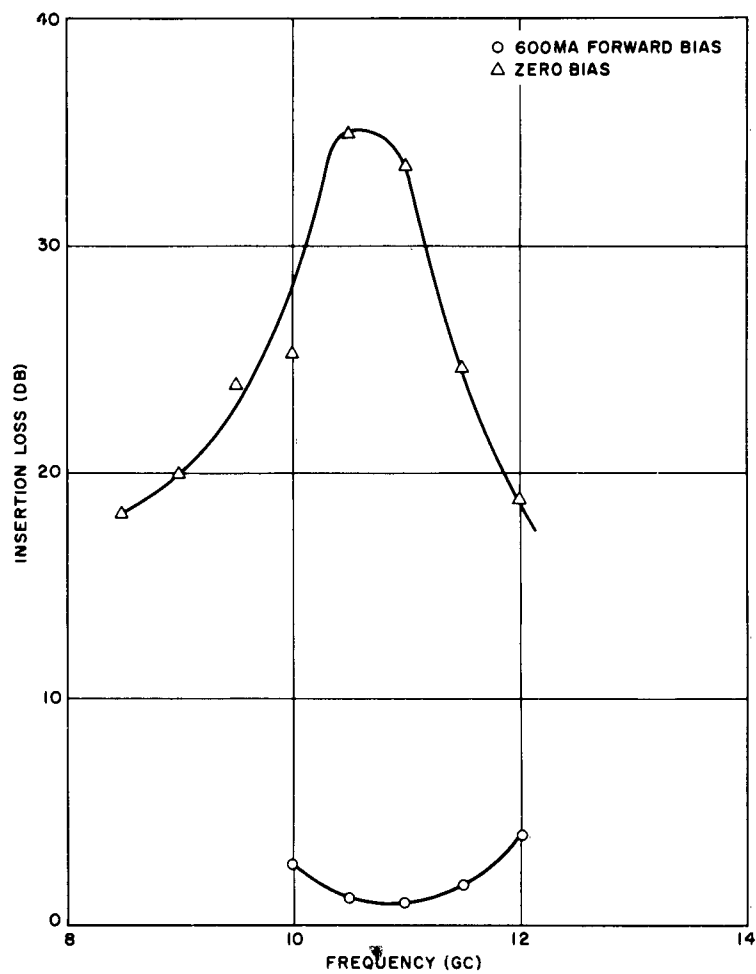


Figure 17. Isolation and insertion loss versus frequency measured for a given diode (showing optimum low level loss and isolation over the same band).

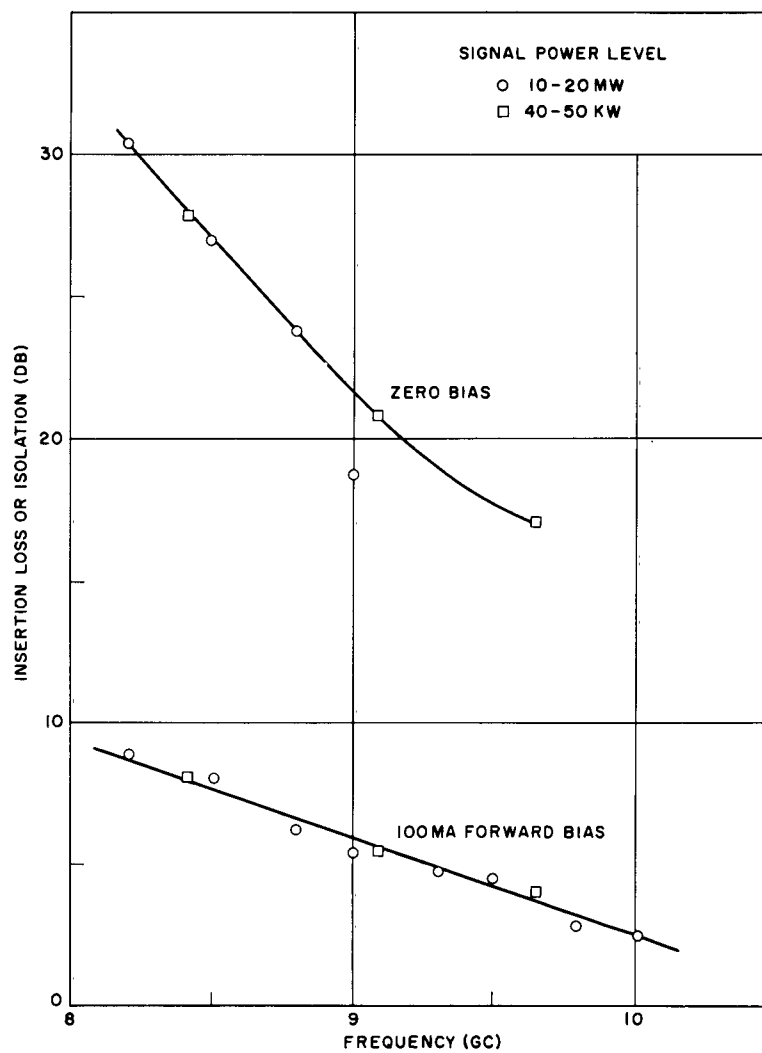


Figure 18. Isolation and insertion loss versus frequency for a given diode measured at low and high power levels (showing that performance is independent of applied power over the range used here).

without external tuning adjustments. The location of the operating frequency band is determined by diode and package reactances; the values of maximum isolation and minimum insertion loss are determined by diode wafer resistance. The more elementary aspects of performance of the switch can be predicted using simple electrical equivalents; these predictions have been verified by measurements. The diode has been shown to switch 50-kilowatt pulses of 2.5-microsecond length without burnout. At these high power levels, values of isolation and insertion loss are in good agreement with those measured at low power. Thus, although the diode had peak voltages of more than 1000 volts across it when it was zero biased, there was no noticeable change in diode impedance resulting from the flow of breakdown current.

#### REFERENCES

1. D. Leenov and R. C. Swenson, "Performance of a Tuned PIN Diode Switch as a Protector for High Power Levels at X-Band," Microwave Diode Research, Report No. 12, Chapter 3 (10 June 1963).
2. R. V. Garver, "Theory of TEM Diode Switching," IRE Trans. on Microwave Theory and Techniques, MTT-9 (May 1961), 224-238.
3. R. V. Garver and D. V. Tseng, "X-Band Diode Limiting," IRE Trans. on Microwave Theory and Techniques, MTT-9 (March 1961), 202.
4. R. V. Garver and J. A. Rosado, "Broad-Band TEM Diode Limiting," IRE Trans. on Microwave Theory and Techniques, MTT-10 (September 1962), 302-310.

## SECTION 5 — CONCLUSIONS

Gold-epitaxial silicon diodes and gold-epitaxial gallium arsenide diodes have been shown to be potentially useful as microwave mixers, fast switches, or varactors. These diodes can be designed and fabricated by large area methods. The series resistance in exploratory models of the Si diodes has been made less than 2 ohms at 100 ma, while the total capacitance at zero bias of the diode plus encapsulation is less than 0.3 picofarad. The cutoff frequency of the GaAs varactor diodes is greater than 150 Gc. For many applications, these diodes may be expected to replace point contact diodes since their greater mechanical and electrical stability, as well as their expected greater reproducibility, makes them more desirable.

A bias-operated PIN diode switch using unencapsulated wafers in a tuned waveguide mount has given 25 to 33 db protection and 0.7-db, low-level insertion loss at X-band. The level of incident power required to produce burnout is estimated to be 14 megawatts for 2.5-microsecond pulses, equivalent to 35-megawatt-microsecond pulse energy. These results are considered sufficiently encouraging to justify further development effort.

A broadband, bias-operated X-band switch using encapsulated PIN diodes and no tuning elements has been explored. Protection greater than 30 db and insertion loss less than 2 db were obtained over a one-Gc band. A diode was able to switch 50-kilowatt pulses of 2.5-microsecond pulse length without burnout. The parasites of the diode package can be utilized in obtaining the necessary resonances. With the achievement of broadband operation, future development effort is needed for the improvement of protection and insertion loss figures.

## SECTION 6 — PROGRAM FOR THE NEXT INTERVAL

The investigation of metal-semiconductor epitaxial diodes will be carried further with the objective of a more complete description of the design of these devices as well as an effort to fabricate higher speed silicon mixer diode, and higher cutoff frequency GaAs varactors.

Analysis of the circuit behavior of Esaki diodes used as microwave amplifiers is continuing.



## SECTION 7 — IDENTIFICATION OF PERSONNEL

The following engineers and scientists have contributed significantly to the work covered in this report.

L. A. D'Asaro  
J. C. Irvin  
D. Kahng  
D. Leenov  
R. C. Swenson

Biographies of Mr. D'Asaro and Mr. Leenov appeared in earlier reports.

### J. C. IRVIN

John C. Irvin received a B. A. degree in physics from Miami University, Oxford, Ohio, in 1949. He worked in the Aircraft Armaments and Optical Laboratories of the Naval Gun Factory, Washington, D. C., during the summers of 1948 and 1949 and entered the Graduate School Physics Department of the University of Colorado in the fall of 1949. He was awarded an M. A. degree by that institution in 1953 and a Ph. D. degree in 1957. During that interval he was employed as both part-time and full-time Instructor at the University. He was the recipient of University Graduate and Research Fellowships and of a Petroleum Research Fund Fellowship (administered by the American Chemical Society). His doctoral dissertation was a theoretical study entitled "Nuclear Quadruple Effects in Internal Rotation." He joined the technical staff of the Bell Telephone Laboratories in July 1957.

He is a member of Sigma Xi, Phi Beta Kappa, and the American Physical Society.

### D. KAHNG

Dawon Kahng received his B. Sc. degree in physics from Seoul University, Seoul, Korea, in 1955 and his M. Sc. and Ph. D. degrees in electrical engineering from Ohio State University in 1956 and 1959 respectively. While at Ohio State University, he was engaged in teaching as well as in the study of diffusion of impurities into silicon through a growing oxide layer. Upon joining the Bell Telephone Laboratories in October 1959, he worked on feasibility studies of surface field effect transistors and hot electron devices and also on silicon epitaxial film doping

profile studies. More recently he has been engaged in the development of surface barrier microwave diodes. He is a member of the Institute of Electrical and Electronics Engineers, Sigma Xi, and Pi Mu Epsilon.

**R. C. SWENSON**

R. C. Swenson served in the United States Air Force as a radar technician from 1951 to 1954. In 1954 he joined the device development group of the Bell Telephone Laboratories. Since then he has been attending evening sessions at Newark College of Engineering, working toward a B. S. degree in electrical engineering. In 1958 he received a junior degree from this college.

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